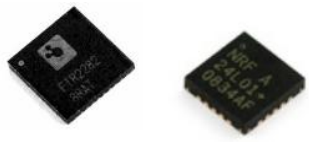
AT3 RF Transceiver Chipset

FEATURES

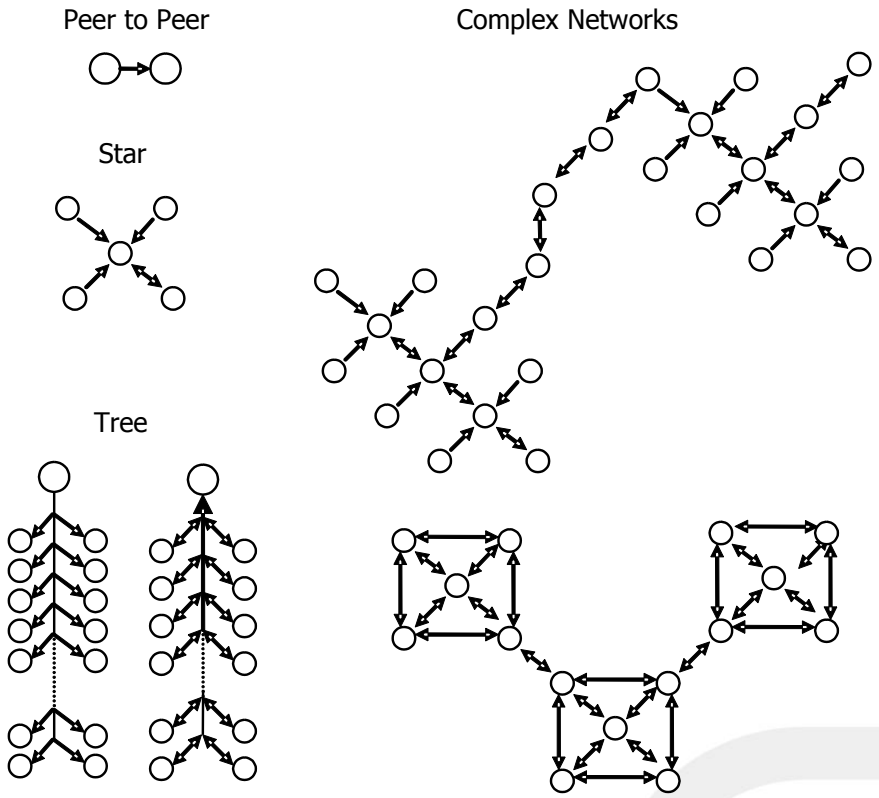
- 2.4GHz worldwide ISM band
- SensRcore™ development platform
- Ultra low power operation
- Simple sync/async serial interface
- Broadcast, Acknowledged, or Burst data transmissions
- 8 byte data payload per message
- Minimum message rate per ANT channel 0.5Hz
- ANT channel combined message rate up to 180Hz
- Burst transfer rate up to 20Kbps (true data throughput)
- 1 Mbps RF data rate
- Up to 1/4/8 ANT channels
- 125 selectable RF channels
- Up to 3 public, managed and/or private networks
- 2.0V to 3.6V supply voltage range
- -40°C to +85°C operating temperature
- RoHS compliant



FAMILY MEMBERS

ANT11TR13: 8 ANT channels
ANT11TS53: 4 ANT channels; SensRcore™
ANT11TS63: 1 ANT channel; SensRcore™

ANT NETWORK CONFIGURATIONS



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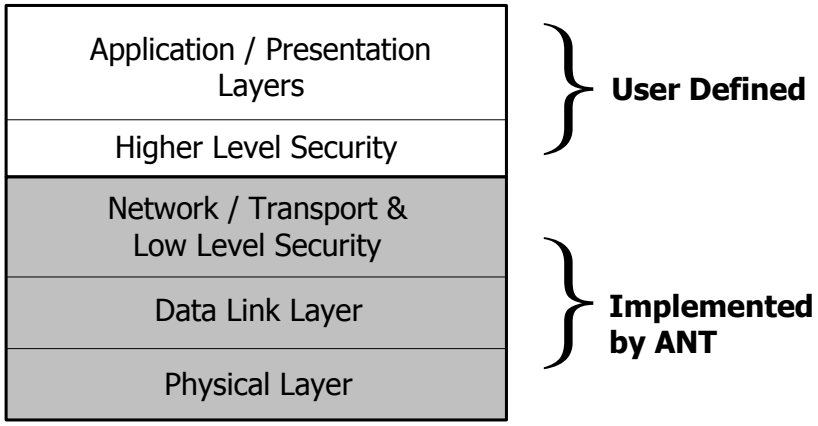
ANT™ Overview

ANT™ is a practical wireless sensor network protocol running on 2.4 GHz ISM band. Designed for ultra low power, ease of use, efficiency and scalability, ANT easily handles peer-to-peer, star, tree and practical mesh topologies. ANT provides reliable data communications, flexible and adaptive network operation and cross-talk immunity. ANT's protocol stack is extremely compact, requiring minimal microcontroller resources and considerably reducing system costs.

ANT provides carefree handling of the Physical, Network, and Transport OSI layers. In addition, it incorporates key low-level security features that form the foundation for user-defined, sophisticated, network-security implementations. ANT ensures adequate user control while considerably lightening computational burden in providing a simple yet effective wireless networking solution.



ANT supports public, managed and private network architectures with 2^{32} uniquely addressable devices possible, ensuring that each device can be uniquely identified from each other in the same network.

ANT is proven with an installed base of over two million nodes in ultra low power sensor network applications in sport, fitness, home and industrial automation. The ANT solutions are available in chips, chipsets and modules to suit a wide variety of application needs.

A complete description of the ANT message protocol is found in the ANT Message Protocol and Usage document. The serial interface details are provided in the Interfacing with ANT General Purpose Chipsets and Modules document.

1 AT3 Chipset

AT3 (ANT11Txx3) chipsets are part of the General Purpose ANT Chipset family. Each chipset comprises an MSP430f2252, the ultra low power microcontroller (MCU) from Texas Instrument, and an nRF24L01 or nRF24L01+, the ultra low power radio chip from Nordic Semiconductor. SensRcore™, an easy-to-use design platform to build wireless sensors, is equipped in most of AT3 chipsets.

AT3 family of chipsets provides a comprehensive solution to the requirements of building a wireless sensor network consisting of nodes from simple sensors to complex hubs or control nodes. Common pin-outs enable easy network development, upgrade, migration and maintenance.

AT3 chipset family has four standard parts:

AT3 Chipset	ANT MCU	Pkg	Radio Chip	Pkg	Description
ANT11TR13	ANTFTR2282	QFN40 6x6mm	nRF24L01 or nRF24L01+	QFN20 4x4mm	8 ANT channels
ANT11TS53	ANTFTS2242	QFN40 6x6mm	nRF24L01 or nRF24L01+	QFN20 4x4mm	4 ANT channels, SensRcore with 6 data channels
ANT11TS63	ANTFTS2212	QFN40 6x6mm	nRF24L01 or nRF24L01+	QFN20 4x4mm	1 ANT channel, SensRcore with 4 data channels

1.1 The ANT MCU

The ANT MCU is an MSP430f2252 embedded with the ANT protocol. It provides the analog and digital inputs and outputs, serial interface to the Host MCU and SensRcore wireless sensor platform.

The serial interface to a host application can be either synchronous or asynchronous. Status and data messages are transferred bi-directionally to create and maintain communication channels, transmit data to and receive data from peripheral sensors and devices. Please refer to ANT Message Protocol and Usage document for details.

1.1.1 SensRcore™ Platform

SensRcore is a wireless sensor development platform that is equipped with most AT3 chipsets. When using sensRcore to develop a wireless sensor, both analog and digital sensors can be directly connected to the ANT MCU. The normally required firmware development is replaced by writing a simple SensRcore script. An application host MCU could be eliminated from the system design. The result is a reduced component cost, size, power and the shortened development cycle of the target sensor device.

When AT3 chipsets are operated in sensRcore mode, the channel configuration parameters are stored in non-volatile memory and are enabled upon power-up. When I/O pins are configured as digital inputs or outputs, the electrical requirements are the same as all other signaling pins. When I/O pins are configured as analog inputs, different signal ranges can be selected with different reference voltages. The reference voltages available are V_{CC}, 2.5V, and 1.5V. Signals that exceed the specified reference level will be read by the A/D as a maximum value. Signal levels should not exceed V_{CC}. Each AIOx pin can be used as an analog input or a digital I/O pin; each IOx pin can be used only as a digital I/O pin. I/O pins that are not being used in a specific SensRcore mode configuration should be left configured as digital inputs, which is the default setting.

ANT sensRcore scripts consist of ANT messages and commands. Please refer to "ANT Message Protocol and Usage" and "SensRcore Messaging and Usage". The script can be generated by using the software tool *SensRware*. There are 200 bytes available in the non volatile memory for SensRcore script.

When developing products, it is recommended to properly leave the access to the ANT MCU serial interface so that SensRcore script can be loaded. Service is provided for volume SensRcore script programming.

1.1.2 Pin-out

The pin-out table for the ANT MCU is specified below. Please refer to the MSP430f2252/4 datasheet for any specific pin requirements.

Pin #	Pin Name	Pin Function	Description
1	DV_{SS}		Digital ground reference
2	XOUT	Output	32.768kHz crystal output
3	XIN	Input	32.768kHz crystal input
4	DV_{SS}		Digital ground reference
5	$\overline{RST}$	Input	Active low reset pin
6	$\overline{SUSPEND}$ /SRDY/AIO0	Input	Async -> Suspend control Sync -> Serial port ready SensRcore Mode -> Analog/Digital input output
7	SLEEP/MRDY/AIO1	Input	Async -> Sleep mode enable Sync -> Message ready indication SensRcore Mode -> Analog/Digital input output
8	TIE_GND1	Input	
9	BR2 / SCLK / DevSel2	Input / Output	Async -> Baud rate selection Sync -> Clock output signal SensRcore Mode -> Configuration selection
10	RF_MOSI	Output	Data output
11	RF_MISO	Input	Data input
12	RF_SCK	Input	SPI clock
13	AV_{ss}		Analog ground reference
14	AV_{CC}		Analog supply voltage
15	IO5	Input	SensRcore Mode -> Digital input output
16	PORTSEL	Input	Asynchronous or Synchronous port select SensRcore Mode -> Demo script or user scripts
17	IO7	Input	SensRcore Mode -> Digital input output
18	TIE_GND2	Input	
19	LED	Output	
20	TIE_GND3	Input	
21	TIE_GND5	Input	
22	TIE_GND4	Input	
23	TXD0/SOUT/IO6	Output	Async -> Transmit data signal Sync -> Data output SensRcore Mode -> Digital input output
24	RXD0/SIN/AIO2	Input	Async -> Receive data signal Sync -> Data input SensRcore Mode -> Analog/Digital output
25	BR1/SFLOW/DevSel1	Input	Async -> Baud rate selection Sync -> Bit or Byte flow control select
26	BR3/DevSel3	Input	Async -> Baud rate selection Sync -> Configuration selection
27	AIO3/VRef-/VeRef	Input/Output	SensRcore Mode -> Analog/Digital output; Negative reference voltage input/output

Pin #	Pin Name	Pin Function	Description
28	AIO4/VRef+/VeRef+	Input/Output	SensRcore Mode ->Analog/Digital Output; Positive reference voltage input/output
29	RTS/SEN/IOSEL	Output	Async -> Request to send Sync -> Serial enable signal SensRcore Mode -> IOSEL tie low
30	TIE_GND6	Input	
31	RF_IRQ	Input	Maskable interrupt pin
32	RF_CE	Output	Radio chip enable
33	RF_CSN	Output	SPI chip select
34	TIE_GND7	Input	
35	TIE_GND8	Input	
36	TIE_GND9	Input	
37	TIE_GND10	Input	
38	DV_{CC}		Digital supply voltage
39	DV_{CC}		Digital supply voltage
40	TIE_GND11	Input	

1.1.3 Asynchronous Baud Rate

The baud rate of the asynchronous communication is controlled by the speed select signals BR1, BR2 and BR3. The table below shows the relationship between the states of the speed select signals and the corresponding baud rates.

BR3	BR2	BR1	Baud Rate
0	0	0	4800
0	1	0	19200
0	0	1	38400
0	1	1	50000
1	0	0	1200
1	1	0	2400
1	0	1	9600
1	1	1	57600

1.1.4 Crystal for clock system

ANT operation requires the 32.768kHz crystal for the MCU clock system meeting the following specification.

Delta F Tolerance	+/- 20ppm @25°C (+/-50ppm Max)
Cl Load Capacitance	11pF (Includes Bond and package capacitance but not PCB capacitance)

1.2 The Radio Chip

The radio chip of AT3 chipset is the nRF24L01 or nRF24L01+ transceiver chip from Nordic Semiconductor. The pin-out of the radio is listed in the Table below. Please refer to the nRF24L01 or nRF24L01+ datasheet for any specific pin requirements.

Pin #	Pin Name	Pin Function	Description
1	RF_CE	Input	Radio chip enable
2	RF_CSN	Input	SPI chip select
3	RF_SCK	Input	SPI clock
4	RF_MOSI	Input	SPI slave data input
5	RF_MISO	Output	SPI slave data output
6	RF_IRQ	Output	Maskable interrupt pin
7	V_{CC}	Power	Power supply
8	V_{SS}	Power	Ground
9	XC2	Analog Output	Crystal pin2
10	XC1	Analog Input	Crystal pin 1
11	V_{CC} _PA	Power	Power supply to power amplifier
12	ANT1	RF	Antenna interface 1
13	ANT2	RF	Antenna interface 2
14	V_{SS}	Power	Ground
15	V_{CC}	Power	Power supply
16	I_{REF}	Analog Input	Reference current
17	V_{SS}	Power	Ground
18	V_{CC}	Power	Power supply
19	DV_{CC}	Power Output	Positive digital supply for de-coupling
20	V_{SS}	Power	Ground

2 Electrical Specifications

NOTE: Please refer to the latest version of MSP430f2252/4 datasheet from Texas Instrument.

NOTE: Please refer to the latest version of the nRF24L01 or nRF24L01+ datasheet from Nordic Semiconductor.

Absolute Maximum Ratings	
Voltage applied at V_{CC} to V_{SS}	-0.3V to +3.6V
Input voltage at any pin	-0.3V to V_{CC} +0.3V
Diode current at any pin	±2mA
Operating temperature	-40°C to +85°C
Storage temperature	-40°C to +105°C

Note: Stress exceeding one or more of the absolute maximum ratings may cause permanent damage to the chipsets.

Conditions: V_{CC} = +2.0V, V_{SS} = 0V, T_A = - 40°C to +85°C

Symbol	Parameter (condition)	Notes	Min	Typ	Max	Units
	Operating conditions					
V_{CC}	Supply voltage		2.2		3.6	V
TEMP	Operating temperature		-40		+85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		1.9		V_{CC}	V
V_{IL}	LOW level input voltage		V_{SS}			V
	Digital output pin					
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		V_{CC} - 0.25		V_{CC}	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		V_{SS}		0.25	V
	Analog input pin					
V_{Analog}	Input voltage range	4)	V_{SS}		V_{CC}	V
F_{Sample}	Sample rate	5)	0.002		500	Sample/s
	Counter input pin					
$F_{Counter}$	Input frequency				1000	Hz
	Synchronous serial timing					
SCLK freq.	Synchronous clock frequency (byte mode)		285	300	315	kHz
$t_{ReadValid}$	Data is valid on read before low-to-high transition on the clock (byte mode)		0.5			µs
$t_{WriteValid}$	Data must be valid on write within this time after a high-to-low transition on the clock (byte mode)				2	µs
t_{SRDY_MinLow}	Minimum $\overline{SRDY}$ low time		2.5			µs
t_{Reset}	Synchronous Reset. $\overline{SRDY}$ falling edge to $\overline{MRDY}$ falling edge		250			µs

Symbol	Parameter (condition)	Notes	Min	Typ	Max	Units
	General RF conditions					
f_{OP}	Operating frequency	1)	2400		2524	MHz
$F_{CHANNEL}$	Channel spacing			1		MHz
Δf	Frequency deviation			±156		kHz
	Current consumption					
I_{Idle}	No active channels – no communications			1.1		µA
$I_{Suspend}$	Asynchronous suspend activated			1.1		µA
I_{Base}	Base active current			2.6		µA
I_{sample}	Average current/analog sample			0.5		µA
$I_{SC\ RF}$	Average current/ ANT message in sensRcore mode			13		µA
$I_{Msg\ Rx\ ByteSync}$	Average current / Rx message in byte sync mode			10.5		µA
$I_{Msg\ Rx\ BitSync}$	Average current / Rx message in bit sync mode			13.1		µA
$I_{Msg\_Rx\_57600}$	Average current / Rx message in Async mode at 57600 baud			9.1		µA
$I_{Msg\_Rx\_19200}$	Average current / Rx message in Async mode at 19200 baud			10.4		µA
$I_{Msg\_Rx\_4800}$	Average RF current / Rx message in Async mode at 4800 baud			8.5		µA
$I_{Msg\_Tx\_ByteSync}$	Average current / Tx-only message in byte sync mode			6.4		µA
$I_{Msg\ Tx\ BitSync}$	Average current / Tx-only message in bit sync mode			10.8		µA
$I_{Msg\_Tx\_57600}$	Average current / Tx-only message in Async mode at 57600 baud			5.7		µA
$I_{Msg\_Tx\_19200}$	Average current / Tx-only message in Async mode at 19200 baud			7.5		µA
$I_{Msg\_Tx\_4800}$	Average current / Tx-only message in Async mode at 4800 baud			4.4		µA
$I_{Msg\_TR\_ByteSync}$	Average current / Tx message in byte sync mode			14.1		µA
$I_{Msg\ TR\ BitSync}$	Average current / Tx message in bit sync mode			18.4		µA
$I_{Msg\_TR\_57600}$	Average current / Tx message in Async mode at 57600 baud			13.5		µA
$I_{Msg\_TR\_19200}$	Average current / Tx message in Async mode at 19200 baud			15.0		µA
$I_{Msg\_TR\_4800}$	Average current / Tx message in Async mode at 4800 baud			11.7		µA
$I_{Msg\_Ack\_ByteSync}$	Average current / Acknowledged message in byte sync mode			19.6		µA
$I_{Msg\_Ack\_BitSync}$	Average current / Acknowledged message in bit sync mode			23.4		µA
$I_{Msg\_Ack\_57600}$	Average current / Acknowledged message in Async mode at 57600 baud			18.7		µA
$I_{Msg\_Ack\_19200}$	Average current / Acknowledged message in Async mode at 19200 baud			19.9		µA
$I_{Msg\_Ack\_4800}$	Average current / Acknowledged message in Async mode at 4800 baud			17.2		µA

Symbol	Parameter (condition)	Notes	Min	Typ	Max	Units
I_{Peak}	Peak Current consumption			19		mA
I_{PeakTx}	Peak Current – Tx-only @ 0dBm			13		mA
I_{Ave}	Broadcast Tx-only @ 0.5Hz in byte sync mode			5.8		µA
I_{Ave}	Broadcast Tx-only @ 2Hz in byte sync mode			15.4		µA
I_{Ave}	Broadcast Rx @ 0.5Hz in byte sync mode			7.8		µA
I_{Ave}	Acknowledged @ 0.5Hz in byte sync mode			12.4		µA
I_{Ave}	Burst continuous @ 14Kbps in byte sync mode			2.24		mA
I_{Ave}	Burst continuous @ 20Kbps in byte sync mode			3.21		mA
I_{Ave}	Burst continuous @ 10Kbps in bit sync mode			3.22		mA
I_{Ave}	Burst continuous @ 14Kbps in Async mode at 57 600 baud			2.37		mA
I_{Ave}	Burst continuous @ 20Kbps in Async mode at 57 600 baud			3.31		mA
	Transmitter operation					
P_{RF}	Maximum output power	2)		0	4	dBm
ΔP	Output power variation	3)			±4	dBm
P_{BW}	20dB bandwidth for modulated carrier				1000	kHz
P_{RF2}	2nd adjacent channel transmit power 2MHz				-20	dBm
P_{RF3}	3rd adjacent channel transmit power 3MHz				-40	dBm
I_{VCC}	Supply peak current @ 0dBm output power			11.3		mA
I_{VCC}	Supply peak current @ -20dBm output power			7		mA
	Receiver operation					
I_{VCC}	Supply peak current receive mode			12		mA
RX_{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-85		dBm
C/I_{CO}	C/I co-channel			9		dB
C/I_{1ST}	1st adjacent channel selectivity C/I 1MHz			8		dB
C/I_{2ND}	2nd adjacent channel selectivity C/I 2MHz			-22		dB
C/I_{3RD}	3rd adjacent channel selectivity C/I 3MHz			-30		dB

1) Usable band is determined by local regulations.
2) Maximum output power with 0dBm output power setting.
3) Variation from 2402MHz to 2479MHz.
4) Voltages exceeding the reference can be used but provide no information.
5) Max refers to total number of samples available to be distributed over the number of A/D sources currently active.

2.1 Current Calculation Examples

1.Master channel with Broadcast data at 4Hz with a bit synchronous serial interface.

$$I_{ave} = (I_{Msg\_Tx\_BitSync} * Message\_Rate) + I_{Base}$$

$$= (18.4\ \mu A/message * 4\ messages) + 2.6\mu A$$

$$= 76.2\ \mu A$$

2.Receive channel with Acknowledged data at 2Hz with an asynchronous serial interface at 57 600 baud.

I_{ave} = ($I_{Msg\_Ack\_57600}$ * Message_Rate) + I_{Base}

= (18.7μA/message * 2 messages) + 2.6μA

= 40.0μA

3.Transmit channel with Acknowledged data at 2Hz with an asynchronous serial interface at 57 600 baud.

I_{ave} = ($I_{Msg\_Ack\_57600}$ * Message_Rate) + I_{Base}

= (18.7 μA/message * 2 messages) + 2.6μA

= 40.0μA

4.SensRcore device using an ANT message rate of 4Hz and sampling an A/D input at 16 Hz.

I_{ave} = (I_{SC_RF} * Message_Rate) + (I_{Sample} * Sample_Rate) + I_{Base}

= (13μA/message * 4 messages) + (0.5μA/sample * 16 samples) + 2.6μA

= 62.6μA

2.2 A/D Specifications

Note: The Tables in Section 2.2 are obtained from Texas Instruments' datasheet.

10-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage range	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage range (see Note 2)	All Ax terminals. Analog inputs selected in ADC10AE register			0		V_{CC}	V
I_{ADC10}	ADC10 supply current (see Note 3)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	I: -40–85°C T: -40–105°C	2.2 V		0.52	1.05	mA
				3 V		0.6	1.2	

10-bit ADC, built-in voltage reference

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	$I_{VREF+} \le 1$ mA, REF2_5V = 0		2.2			V
		$I_{VREF+} \le 0.5$ mA, REF2_5V = 1		2.8			
		$I_{VREF+} \le 1$ mA, REF2_5V = 1		2.9			
V_{REF+}	Positive built-in reference voltage	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0	2.2 V/3 V	1.41	1.5	1.59	V
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1	3 V	2.35	2.5	2.65	

10-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		2.2 V/3 V			±1	LSB
E_D	Differential linearity error		2.2 V/3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω,	2.2 V/3 V			±1	LSB
E_G	Gain error	SREFx = 010, unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±1.1	±2	LSB
		SREFx = 010, unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±1.1	±2	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 1.5 V	2.2 V		±1.1	±4	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 2.5 V	3 V		±1.1	±3	
E_T	Total unadjusted error	SREFx = 010, unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±2	±5	LSB
		SREFx = 010, unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±2	±5	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 1.5 V	2.2 V		±2	±7	
		SREFx = 011, buffered external reference (see Note 1), V_{eREF+} = 2.5 V	3 V		±2	±6	

NOTES: 1. The reference buffer offset adds to the gain and total unadjusted error.

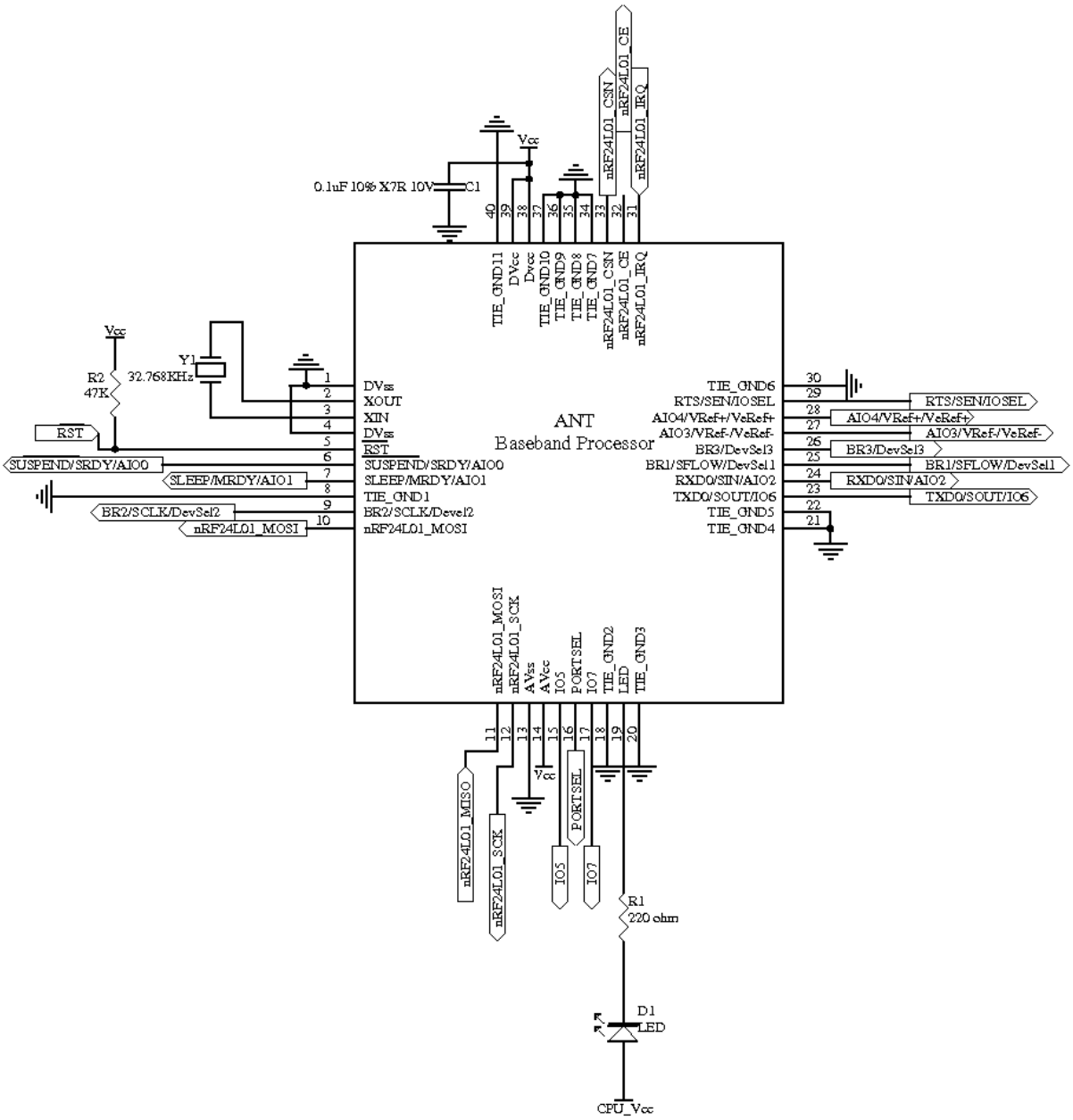
10-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference input voltage range (see Note 2)	$V_{eREF+} > V_{eREF-}$, SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		$V_{eREF-} \le V_{eREF+} \le V_{CC}$ – 0.15 V, SREF1 = 1, SREF0 = 1 (see Note 3)		1.4		3.0	
V_{eREF-}	Negative external reference input voltage range (see Note 4)	$V_{eREF+} > V_{eREF-}$		0		1.2	V
ΔV_{eREF}	Differential external reference input voltage range $\Delta V_{eREF} = V_{eREF+} - V_{eREF-}$	$V_{eREF+} > V_{eREF-}$ (see Note 5)		1.4		V_{CC}	V
I_{VeREF+}	Static input current into V_{eREF+}	0V ≤ V_{eREF+} ≤ V_{CC}, SREF1 = 1, SREF0 = 0	2.2 V/3 V			±1	µA
		0V ≤V_{eREF+} ≤ V_{CC} – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 (see Note 3)				0	
I_{VeREF-}	Static input current into V_{eREF-}	0V ≤ V_{eREF-} ≤ V_{CC}	2.2 V/3 V			±1	µA

NOTES:
1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. Under this condition, the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
4. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
5. The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

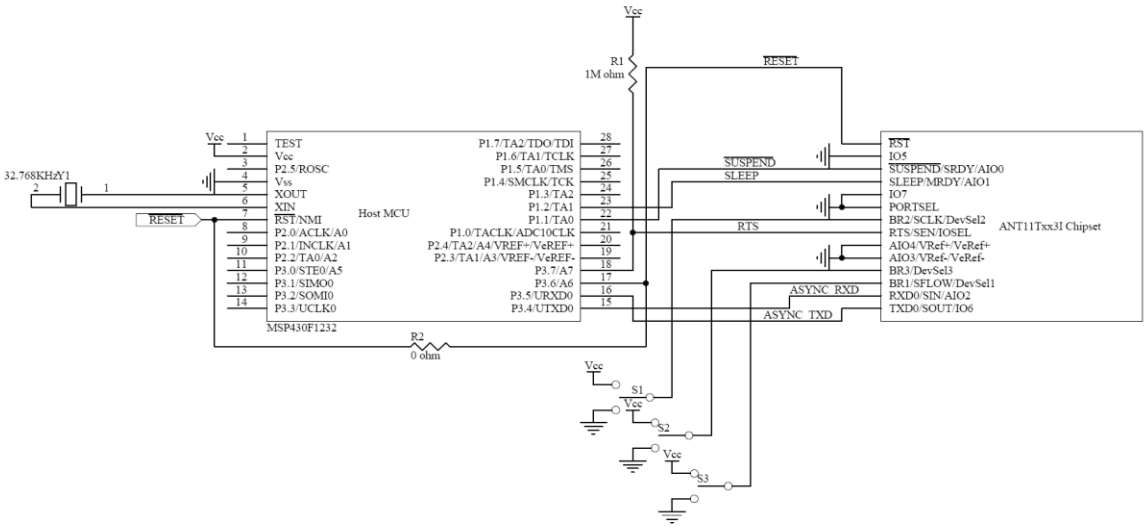
3 Schematics

3.1 ANT Baseband Processor Schematic



3.2 Interface Examples

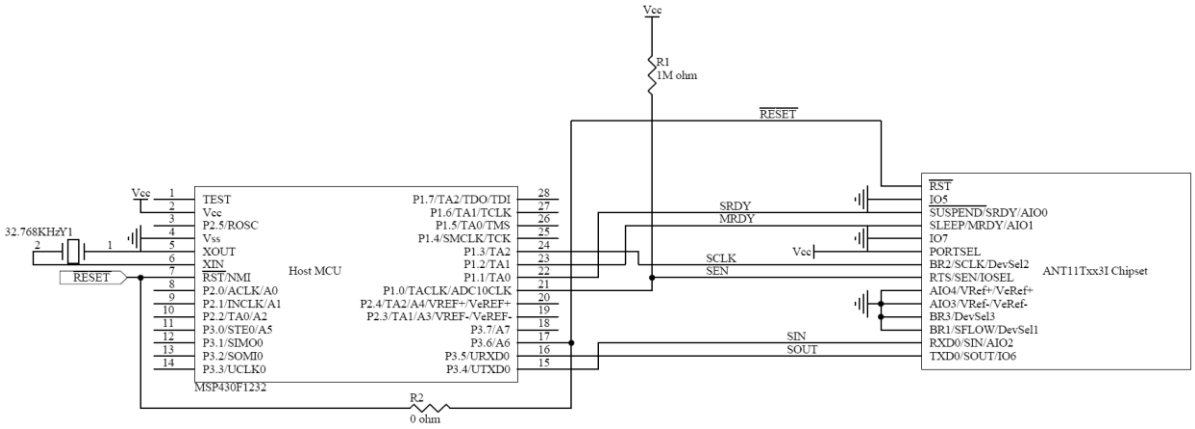
3.2.1 Async Mode



Notes:

- The ANT chipset's RXD and TXD connected directly to hardware USART of microcontroller.
- The illustrated switches on the baud rate selection pins (BR1, BR2, and BR3) are for ease of use only. The Baud rate selection pins may be connected directly to the logic level of interest.
- R2 allows optional control of the ANT chipset's $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

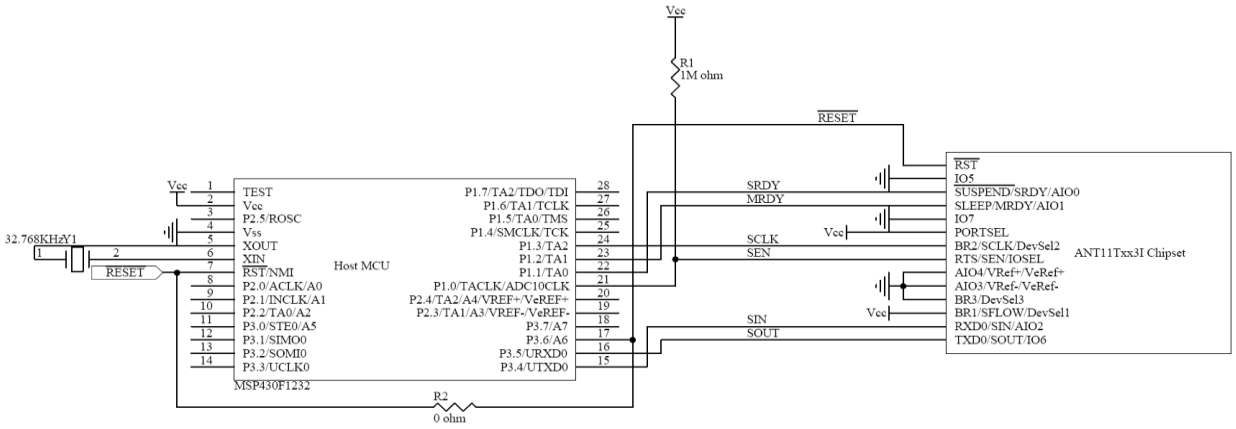
3.2.2 Byte Sync Mode



Notes:

- The ANT chipset's SOUT and SIN connected directly to hardware USART of microcontroller.
- SCLK and SEN need to be on interrupt-capable I/O pins on the microcontroller.
- R3 allows optional control of the ANT chipset's $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

3.2.3 Bit Sync Mode



Notes:

- All interface signals are connected directly to I/O pins on the microcontroller.
- SCLK and SEN need to be on interrupt-capable I/O pins on the microcontroller.
- R3 allows optional control of the ANT chipset's $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.