AT3 Chipset Errata

D00001452 Rev 1.0

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This document describes the known exceptions to the datasheet of AT3 chipsets. Workarounds or fixes are provided.

1 Chipset Revision

The AT3 chipsets contains two chips, an ANT MCU and an Radio IC nRF24L01 or L01P from Nordic Semiconductor. The chipset revision refers to the firmware version loaded to the ANT MCU. It can be identified in the following ways.

1.1 ANT MCU Tracking Code

Each AT3 MCU has a 4 character tracking code printed on the product sticker. The third character denotes the revision. The picture shows that the ANT MCU is rev B.

1.2 Package Label

For sealed reels, the revision is marked on the package Label as below

1.3 Version String

In the case that the chip sticker is hard to access or identification marker is blurred, an ANT version command 0x3E can be issued via the serial communication to acquire the version String.

Revision	Version String
B	AGC1.05Cxx [1]
A	AGC1.04Cxx [1]

Note 1: "xx" denotes the different AT3 model. For the 8 channel, non-SensRcore FTR2282, it shows 'AD"

2 Known Issues

2.1 Multiple Channel Collision

Rev A is affected. This issue has been fixed in rev B and above

Symptoms: Having multiple channels on a single device with at least one master can cause prolonged blocked channel events and in some cases a channel outage of 2 seconds or more resulting in long data outages or searches on the slave device.
Conditions: Channels of different message rates are opened on the same device, one being a master channel. The message rates are not synchronous relative to each other and thus collide over time.
Consequences: Channel collision is unavoidable in this case of multiple channels at different message rate. But the issue causes higher than normal failures. In some instances, this causes a 2 second outage for a master channel, which can result in the slave device dropping to search.
Workaround: If the multi-channel scenario is one master and some number of slaves, using channel 0 for the master channel can mitigate the issue.

2.2 Initialization Issue After a Reset

Both rev A and Rev B are affected. This issue will be fixed in rev C

Symptoms: The AT3 chipset sometimes fails to initialize after a reset.
Conditions: This issue is seen when an external clock source is used. Failure points can vary from chip to chip. The issue does not appear when using a crystal as the clock.
Consequences: Chipset may fail to initialize sporadically after a reset.
Workaround: Use the RESET pin to reset the chipset, and retry the reset sequence if the AT3 fails to initialize properly after a reset. A successful initialization can be confirmed by observing the AT3 lowering RTS within 500ms of a reset. The phase of the reset pulse with respect to the external clock source should be different in each reset retry attempt.